

WHAT IS CLAIMED IS:

1 1. In an integrated circuit multiprocessor switching device, an apparatus for
2 transferring data from a first bus to a memory bus, comprising:
3 a first interface circuit for receiving packet data and transferring the packet data to
4 a first bus having a first data width;
5 a memory bus having a second data width that is larger than the first data width;
6 a packet manager circuit coupled between the first bus and the memory bus to
7 transfer data received from the first interface circuit to memory under control of at least a
8 first descriptor, said packet manager circuit comprising,
9 an input buffer coupled to the first bus;
10 an alignment circuit coupled to the input buffer for shifting data stored in the
11 input buffer to output shifted data; and
12 a controller for controlling the shifting of data in the alignment circuit in response
13 to an offset contained in the first descriptor and for writing the shifted data to the memory
14 bus.

1 2. The apparatus recited in claim 1, comprising a data merge circuit coupled
2 to store in a fragment storage register the shifted data from the alignment circuit that is
3 not written to memory in a first data cycle, said data merge circuit combining data stored
4 in the fragment storage register with data stored in the input buffer in a second data cycle
5 to form a merged data value that is written to the memory bus.

1 3. The apparatus recited in claim 2, wherein the merged data value has a data
2 width equal to the first data width.

1 4. The apparatus recited in claim 2, wherein the merged data value has a data
2 width equal to the second data width.

1 5. The apparatus recited in claim 1, wherein the input buffer comprises FIFO
2 buffer.

1 6. The apparatus recited in claim 1, where the alignment circuit comprises a
2 fragment storage buffer for storing a portion of a first packet fragment that has been
3 stored in the input buffer and shifted to create a first data fragment, whereby the first data
4 fragment is merged with a portion of a second packet fragment that has been stored in the
5 input buffer and shifted to create a second data fragment.

1 7. The apparatus recited in claim 1 for transferring data on a plurality of
2 channels from the first bus to the memory bus, where the input buffer comprises a buffer
3 region for each of the plurality of channels.

1 8. The apparatus recited in claim 7, where the packet manager circuit uses
2 register files for storing intermediate values of packets and states for the plurality of
3 channels.

1 9. In a packet manager circuit, an apparatus for aligning and merging packet
2 fragments for storage in or transfer from memory under control of at least a first
3 descriptor, comprising:
4 an input buffer for receiving packet fragments having a first data width;
5 an output buffer having a second data width; and
6 a data alignment circuit coupled between the input buffer and the output buffer for
7 aligning the packet fragments to an offset specified in at least a first descriptor and
8 combining said aligned packet fragments for storage in said output buffer by storing a
9 data fragment from said combined aligned packet fragments in a fragment storage buffer.

1 10. The apparatus recited in claim 9, comprising a packet manager input
2 circuit where the input buffer comprises a FIFO register and the output buffer comprises
3 a memory buffer having a data width that is larger than the first data width.

1 11. The apparatus recited in claim 9, comprising a packet manager output
2 circuit where the output buffer comprises a FIFO register having a data width that is
3 smaller than the first data width.

1 12. The apparatus recited in claim 9, where the data alignment circuit
2 comprises:

3 a first fragment storage register for storing a first shifted data value from a first
4 data beat;

5 a second fragment storage register for storing a first fragment data value from the
6 first data beat;

7 a data shifter coupled to the input buffer for generating the first shifted data value
8 and first fragment data value during the first data beat and for generating a second shifted
9 data value during a second data beat; and

10 a selection circuit combining the first shifted data value, first fragment data value
11 and second shifted data value into a merged data value for storage in the output memory
12 buffer.

1 13. The apparatus recited in claim 10 for storing packet fragments in a
2 plurality of channels, where the FIFO register comprises a read pointer and write pointer
3 for each channel.

1 14. The apparatus recited in claim 9, comprising a packet manager output
2 circuit where the input buffer comprises a plurality of data buffers for storing at least part
3 of a packet stored in memory and the output buffer comprises a FIFO buffer having a
4 data width that is smaller than the first data width.

1 15. The apparatus recited in claim 9, where the input buffer comprises first
2 and second storage buffers for storing a data received from memory; where the output
3 buffer comprises a FIFO output buffer for holding aligned output data values; and where
4 the data alignment circuit comprises:

5 a data shifter selectively coupled to the first and second storage buffers for
6 generating the first shifted data value and first fragment data value during a first data beat
7 and for generating a second shifted data value during a second data beat;

8 a fragment storage buffer for accumulating data values from the data shifter; and

9 a selection circuit combining shifted data values from the fragment storage buffer
10 and data shifter into an aligned output data value for storage in the FIFO output memory
11 buffer.

1 16. A method for aligning and merging packet data received on at least a first
2 channel from a first bus to a second bus in an integrated circuit, comprising:
3 receiving from the first bus a first input data having a first line width;
4 shift rotating the first input data to generate a first shifted data and a first fragment
5 data;
6 receiving from the first bus a second input data having the first line width;
7 shift rotating the second input data to generate a second shifted data and a second
8 fragment data;
9 merging the first shifted data, first fragment data and second shifted data into an
10 output data for transmission to the second bus.

1 17. The method of claim 16, where the second bus has a line width that is at
2 least twice as large as the first line width.

1 18. The method of claim 16, where the second bus has a line width that is
2 smaller than the first line width.

1 19. The method of claim 16, comprising
2 shift rotating the first input data under control of an offset value contained in a
3 first descriptor;
4 storing the first shifted data in a first storage register during a first data beat;
5 storing the first fragment data in a second storage register during a first data beat;
6 and
7 merging the first shifted data, first fragment data and second shifted data by
8 selectively combining the first shifted data, first fragment data and second shifted data
9 and transferring the combined data over the second bus to a memory buffer under control
10 of said first descriptor.

1 20. The method of claim 16, where packet data on a plurality of channels is
2 aligned and merged by storing in a register file, for each channel, intermediate values for
3 each packet data